CLAIMS

Please amend the claims as follows.

1. (Currently amended) A testing circuit for thin film transistor display array testing, use to test the yield of thin film transistor display array, comprising:

An array tester, providing electrical power, testing signal wave- form, for analyzing, calculating, storing [[the]] testing results;

A device under test (DUT) platform, for holding the thin film transistor display array, and providing control signal to the platform and [[the]]a sense amplifier by the array tester;

A sense amplifier array, for transferring (discharge) the parasitic capacitance of the source line of the thin film transistors and integrating [[the]] charge current of a pixel storage capacitor~~, wherein the improvement comprising~~:

wherein [[Said]]said sense amplifier array is composed by a plurality of trans-impedance amplifier units and a plurality of parasitic capacitance discharge circuits, ~~every~~the sense amplifier array including:

A trans-impedance amplifier, is composed by [[an]]a first operational amplifier, ~~two switches~~a first switch, a second switch and [[an]]a first operation capacitor; said first operation capacitor feed back the output of the first operational amplifier to the negative input of the first operational amplifier; [[a]]the first switch connecting to the output and negative input of the first operational amplifier, to short circuit the first operation capacitor for discharge; ~~another~~the second switch to be the input switch, to connect or disconnect with the pixel storage capacitor; said trans-impedance amplifier forms an integrated circuit, the output of the first operational amplifier is transmitted to a sampling/hold circuit via an output switch and converted to a digital signal;

A discharge circuit for the parasitic capacitance of the source line of the thin film transistors, composed by a second operational amplifier, ~~two switches~~a third switch, a

fourth switch and [[an]]a second operation capacitor; said second operation capacitor feed back the output of the second operational amplifier to the negative input of the second operational amplifier; [[a]]the third switch connecting to the output and negative input of the second operational amplifier, to short circuit the second operation capacitor for discharge; ~~another~~the fourth switch to be the input switch, to connect or disconnect with the parasitic capacitance of the source line of the thin film transistors; a load resistance connecting the output of [[said]]the second operational amplifier to the ground; said discharge circuit forms a discharge route for the parasitic capacitance.

2. (Currently amended) A testing circuit as recited in claim 1, wherein said thin film transistor display array is liquid crystal display (LCD) panel.

3. (Currently amended) A testing circuit as recited in claim 1, wherein said thin film transistor display array is organic light emitting diode display (OLED) panel.

4. (Currently amended) A testing circuit as recited in claim 1, wherein said thin film transistor display array is LCOS (liquid crystal on silicon) panel.

5. (Currently amended) A testing circuit as recited in claim 1, wherein said thin film transistor display array is formed by amorphous thin film transistors.

6. (Currently amended) A testing circuit as recited in claim 1, wherein said thin film transistor display array is formed by poly-Si thin film transistor.

7. (Currently amended) A testing circuit as recited in claim 1, wherein said thin film transistor display array is formed by re-crystallized silicon thin film transistor.

8. (Currently amended) A testing circuit as recited in claim 1, wherein said amplifier is an operational amplifier.

9. (Currently amended) A testing circuit as recited in claim 1, wherein said first, second, third and fourth switches are control by the programmable output waveform of said array tester.

10. (Original) A testing circuit as recited in claim 1, wherein the capacitance of said operation capacitor of said trans-impedance amplifier is 1 pf to 100pf.

11. (Original) A testing circuit as recited in claim 1, wherein the capacitance of said operation capacitor of said discharge circuit is greater than 10 pf.

12. (Currently amended) A testing method for invalid pixel (invisible area) of thin film transistor display array, comprising the steps of:

Charging the pixel storage capacitors of [[the]] nth column of the ~~device under test~~thin film transistor display array through a pixel switch transistors to a charge voltage of V_S, then open circuit the pixel switch transistors after charging;

Switching ON [[the]] short circuit switches of [[the]] sense amplifiers and [[the]] discharge circuits to discharge the operation capacitors of the sense amplifiers and the discharge circuits;

Switching ON [[the]] input switches of the discharge circuits; switching OFF [[the]] short circuit switches to discharge the parasitic capacitance of the thin film transistor display array (transferring the charge)~~, the transferring time is longer~~;

Switching ON [[the]] input switches of the sense amplifiers to start operation of

the sense amplifier, integrating [[the]]any current from [[the]]a pixel storage capacitor of column n and row k, but do not output the result of the integrated current;

Testing [[the]]a next pixel (column n and row (k+1)).

13. (Currently amended) A testing method for valid pixel (visible area) of thin film transistor display array, comprising the steps of:

Charging the pixel storage capacitors of [[the]] nth column of the ~~device under test~~thin film transistor display array through a pixel switch transistors to a charge voltage of V_s, then open circuit the pixel switch transistors after charging;

Switching ON [[the]]short circuit switches of [[the]]sense amplifiers and [[the]]discharge circuits to discharge the operation capacitors of the sense amplifiers and the discharge circuits;

Switching ON the input switches of [[the]] sense amplifiers to start operation of the sense amplifier, integrating [[the]]any current from [[the]]a pixel storage capacitor of column n and row k, [[the]]to integrate a voltage [[is]] Vd;

Switching ON the input switches of [[the]] discharge circuits; switching OFF the short circuit switch of discharge circuits to discharge the parasitic capacitance of the thin film transistor display array (transferring the charge), for [[the]] testing of [[the]]a next pixel~~, the transferring time is shorter~~;

Testing the next pixel (column n and row (k+1)).

14. (Original) A testing method as recited in claim 12 or 13, wherein said charging voltage V_s of the pixel capacitors is 2 Volts to 10 Volts.

15. (Original) A testing method as recited in claim 13, wherein said integrated voltage $V_{[[s]]d}$ is greater than 100 mV.